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DATE: Thursday, January 18, 2007 **Purge Queries** Printable Copy Create Case

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L9: Entry 2 of 5 File: USPT Mar 28, 2006

DOCUMENT-IDENTIFIER: US 7020000 B2
** See image for Certificate of Correction **
TITLE: Reducing power dissipation in a match detection circuit

PRIOR-PUBLICATION:

DOC-ID	DATE
US 20050135136 A1	June 23, 2005

Description Paragraph (19):
During operation of match detection circuit 275, the Matchline 185 is precharged to Vcg. If a match is detected between the input bit (e.g., MBIT) and its corresponding stored bits (e.g., Q), then the Matchline 185 remains at a logic HIGH level (i.e., Vcg). If a mismatch is detected between the input bit and the stored bit, then the Matchline 185 is discharged from Vcg to ground.

Description Paragraph (20):
Significantly, when the Matchline 185 voltage is discharging from Vcg to ground, eventually, the Matchline voltage will discharge to a level just below the threshold voltage (e.g., approximately 0.75V, depending on the technology used) of the p-type transistor through which the Matchline 185 is being discharged (e.g., 205, 240). The p-type transistor (e.g., 205, 240) then cuts off and no longer conducts. That is, the threshold voltage (e.g., 0.75V) becomes the voltage level associated with a logic LOW state when a mismatch is detected. In accordance with this embodiment of the invention, the voltage swing is limited to Vcg-Vthreshold (Vth), thereby significantly reducing the power dissipated by the match detection circuit 275.

Description Paragraph (25):
Turning to FIG. 5, a schematic diagram of a CAM match detection circuit 575 is depicted in accordance with another exemplary embodiment of the invention. In this configuration, the Matchline 585 is located at the lower portion of the circuit and is coupled to the ground terminal (e.g., VSS) via precharge transistor 510. Here, the Matchline 585 is precharged to VSS via p-type precharge transistor 510. It should be noted that if precharge transistor 510 is an n-type transistor, a Precharge signal, rather than the Precharge_N signal, would be used. When a match is detected between the input bit and the stored bit, the Matchline remains at logic LOW (e.g., VSS), thereby signifying that a match has been detected. When a mismatch is detected, the voltage on the Matchline is increased from VSS to VDD.

Description Paragraph (26):
Significantly, transistors 505 and 500 are n-type transistors having their respective sources coupled to the Matchline 585. As a result, when a mismatch is detected, as is the case most of the time, the Matchline 585 voltage increases only as far as the threshold voltage (e.g., 0.75V) of the transistors 505, 500. Once the threshold voltage is reached, the transistors 505, 500 are cut off and stop conducting. The threshold voltage is then considered to be the logic HIGH state which signifies a mismatch on the Matchline 585. Consequently, the Matchline voltage swing is reduced to Vth-VSS since the Matchline 585 voltage never reaches VDD and the overall power dissipation of the match detection circuit 575 is greatly reduced.

Description Paragraph (30):
In CAM match detection circuit 875, the stored bit is compared with the input bit on the MBIT_N line. The stored bit is coupled to the gate of transistor 110 and the incoming

bit, MBIT_N, is coupled to the gate of transistor 505. First, the Matchline 885 is precharged to VSS. If a match is detected, the Matchline 885 is not coupled to VDD, via at least one pair of series connected transistors (e.g., 110 and 505) and the Matchline 885 remains at VSS, thus signifying that a match was detected. If a mismatch is detected, then the Matchline 885 will be coupled to VDD and the Matchline voltage will rise toward VDD.

Description Paragraph (35):
With reference to the above, FIG. 9 depicts a match detection circuit 975 having a source coupled CAM cell 950 similar to that of FIG. 2 coupled to a Matchline Voltage Reference Generator (Generator) 960. The Generator 960 generates and regulates Vcg so that Vcg is maintained at an optimal level for reducing power dissipation while still enabling detection of a match condition versus a mismatch condition.

Description Paragraph (49):
It is desirable to have a CAM match detection circuit that dissipates less power while maintaining traditionally achieved levels of performance. The present invention accomplishes this by providing match detection circuits that reduce the magnitude of signal swing when a mismatch is detected. As illustrated by several exemplary embodiments of the invention, the Matchline voltage swings from the precharge voltage (e.g., Vcg) to VSS. In addition, p-type transistors are used with their sources coupled to the Matchline, thereby further limiting the voltage swing when the Matchline is discharged toward VSS. The reduced voltage swing during match detection greatly reduces the power dissipated by the match detection circuits.

CLAIMS:

1. A method for detecting a mismatch in a content addressable memory (CAM), the method comprising: charging a matchline of a match detection circuit of said CAM to a first voltage level lower than a supply voltage level; comparing a logic state of a first bit stored in said CAM with a logic state of a second bit received at said CAM, said comparison comprising receiving said logic state of said first bit at a gate of a first transistor, and receiving said logic state of said second bit at a gate of a second transistor in series with said first transistor, wherein if said logic state of said first bit does not match said logic state of said second bit, said first and second transistors are activated and conducting; and changing the voltage level of said matchline to a ground voltage level through said first and second transistors if the logic state of the first bit does not match the logic state of the second bit.

4. A method for detecting a mismatch in a content addressable memory (CAM), the method comprising: charging a matchline of a match detection circuit of said CAM to a supply voltage level; comparing a logic state of a first bit stored in said CAM with a logic state of a second bit received at said CAM, said act of comparing comprising receiving said logic state of said first bit at a gate of a first transistor coupled to said matchline; and receiving said logic state of said second bit at a gate of a second transistor in series with said first transistor, wherein if said logic state of said first bit does not match said logic state of said second bit, said first and second transistors are activated and conducting; discharging the voltage level of said matchline through said first and second transistors from said supply voltage level to a threshold voltage of said first transistor coupled to said matchline if the logic state of the first bit does not match the logic state of the second bit; and detecting said mismatch based on the change in voltage level of said matchline from said supply voltage level to said threshold voltage level.

7. A method for detecting a mismatch in a content addressable memory (CAM), the method comprising: charging a matchline of a match detection circuit of said CAM to a first voltage level lower than a supply voltage level; comparing a logic state of a first bit stored in said CAM with a logic state of a second bit received at said CAM; and discharging the voltage level of said matchline from said first voltage level to a threshold voltage of a transistor coupled to said matchline if the logic state of the first bit does not match the logic state of the second bit; detecting said mismatch based on the change in voltage level of said matchline from said first voltage level to said threshold voltage level.

12. A method for detecting a mismatch in a content addressable memory (CAM), the method comprising: charging a matchline of a match detection circuit of said CAM to a ground voltage level; comparing a logic state of a first bit stored in said CAM with a logic state of a second bit received at said CAM; and changing the voltage level of said matchline to a voltage level greater than said ground voltage level if the logic state of the first bit does not match the logic state of the second bit; and detecting said mismatch based on the change in voltage level of said matchline from said ground voltage level to said voltage level greater than said ground voltage level.

18. A match detection circuit for a content addressable memory (CAM), comprising: a circuit for precharging a matchline to a first voltage level lower than a supply voltage level; and a circuit for switchably coupling said matchline to a second ground voltage terminal through first and second transistors in series, for changing a logic state of said matchline when a logic state of a first stored bit of said CAM does not match a logic state of a second received bit of said CAM.

23. A semiconductor memory chip, comprising: a plurality of match detection circuits for a content addressable memory (CAM), each of said match detection circuits comprising: a matchline configured to be precharged by a first voltage terminal to a first voltage level lower than a supply voltage level; and a circuit for switchably coupling said matchline to a second ground voltage terminal through first and second transistors in series, for changing a logic state of said matchline if a logic state of a first stored bit of said CAM does not match a logic state of a second received bit of said CAM.

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L9: Entry 3 of 5 File: USPT Feb 21, 2006

DOCUMENT-IDENTIFIER: US 7002823 B1

**** See image for Certificate of Correction ****

TITLE: Content addressable memory with simultaneous write and compare function

Description Paragraph (71):

Returning to FIG. 6, the compare circuit 208 compares the output of the parity generator 206 with the corresponding stored parity bit. Compare circuit 208 is preferably a combinatorial logic circuit such as an XOR circuit that outputs a logic `1` only if the stored parity bit and the parity bit generated by the parity generator 206 do not match, but may alternatively be any type of circuit for detecting mismatch between the stored and generated parity bits. The outputs of all the compare circuits 208 are logically ORed in gate 221 so that, if any one of the compare circuits 208 signals a mismatch (i.e., a logical `1`), the parity check circuit 201 will output a logical `1`. For embodiments in which a single parity bit is used for an entire CAM word, OR gate 221 may be omitted. As shown in FIG. 6, the output of the parity check circuit 201 is gated by the validity bit for the CAM word in AND gate 222 to generate a parity error signal 231. That is, even if a parity mismatch is signaled by the parity check circuit 201, the parity error signal 231 will not be asserted by AND gate 222 unless the validity bit for the CAM word being error checked indicates that the CAM word is valid. By this arrangement, parity errors are signaled only for valid CAM words.

Description Paragraph (165):

Still referring to FIG. 31, the compare circuit 910 includes transistors 911, 912, 913 and 914. Transistors 911 and 912 are coupled in series between a match line 827 and a reference potential (ground in this example), with a gate terminal of transistor 911 being coupled to receive the data value from storage element 901 and a gate terminal of transistor 912 being coupled to receive a complemented comparand bit from comparand line {overscore (CL)}. Similarly, transistors 913 and 914 are coupled in series between the match line 827 and the reference potential, with a gate terminal of transistor 913 being coupled to receive a complemented version of the data value stored in storage element 901, and a gate terminal of transistor 914 being coupled to receive an uncomplemented comparand bit from comparand line CL. By this arrangement, if the comparand value and the stored data value do not match, the match line 827 will be pulled low through one of the transistor pairs 911/912 or 913/914, thereby signaling the mismatch condition. For example, if the comparand is high and the stored data value is low, then transistors 913 and 914 will be switched on to pull the match line 827 low. Conversely, if the comparand is low and the stored data value is high, transistors 911 and 912 will be switched on to pull the match line 827 low. If the comparand and data value match, then neither transistor pair 911/912 nor 913/914 will be fully switched on, thereby interrupting the path to the reference potential (so that the match line is not pulled low) to indicate the match condition. It should be noted that additional circuitry may be included within the CAM cell 801, including without limitation, timing control circuitry interposed between the ground reference and source terminals of transistors 912 and 914 of the compare circuit 910 to provide for timing control over the comparison of the comparand value and stored data value. Further, although a specific compare circuit implementation has been described in reference to FIG. 31, any other circuit that may be used to detect a match condition (or mismatch condition) may be used in alternative embodiments.

CLAIMS:

16. The method of claim 15 wherein outputting a signal that indicates a mismatch between contents of the selected row and the comparand value comprises switchably coupling a match line to a first reference voltage, the match line corresponding to the selected

row.

17. The method of claim 15 wherein switchably coupling the match line to the first reference voltage comprises switchably coupling the match line to ground.

18. The method of claim 15 wherein switchably coupling the match line to the first reference voltage comprises coupling the match line to the first reference voltage in response to the word line being activated.

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